a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and

a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive wiring line structure is above the subtractive etch metallic cap and is conductively coupled to the subtractive etch metallic cap.

REMARKS

Claims 1-14 and 29-42 are currently pending based on the amendment herein, wherein claims 15-28 have been cancelled, claim 1 has been amended, and claims 29-44 are new.

The Examiner alleged that "Figures 1-3E should be designated by a legend such as -- **Prior Art**-- because only that which is old is illustrated. See MPEP §608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance." In response, Applicants have amended the drawings.

The Examiner rejected claims 1-7 and 9-14 under 35 U.S.C. §103(a) "as being unpatentable over Prior Art Figures 1-3E in view of Farooq *et al.* (5,705,857)."

The Examiner rejected claim 8 under 35 U.S.C. §103(a) "as being unpatentable over Prior Art Figures 1-3E in view of Farooq *et al.* (5,705,857) as applied to claim 1 above, and further in view of Cheek et al. (6,018,180)."

Applicants respectfully traverse the 35 U.S.C. §103 rejections with the following arguments.

35 U.S.C. §103

The Examiner alleges that "Prior Art Figures 1-13E teach an electronic structure 10, comprising: a substrate layer 12 that includes a first electronic device 20; a first insulative layer 48 on the substrate layer; a first damascene conductive wire/stud 61 having a lower portion in the first insulative layer and an upper portion above the first insulative layer; a second insulative layer 7 on the first insulative layer; a damascene conductive wiring line structure 8 within the second insulative layer; the lower portion of the first damascene conductive wire/stud is conductively coupled to a first portion 23 of the first electronic device; a second damascene conductive wire/stud 62 having a lower portion in the first insulative layer and an upper portion above the first insulative layer, wherein the lower portion of the second damascene conductive wire/stud is conductively coupled to a second portion 22 of the first electronic device; the first electronic device being a MOS field effect transistor (FET), wherein the first portion of the first electronic device includes a gate of the FET, and wherein the second portion of the first electronic device is selected from the group consisting of a source of the FET and a drain of the FET; the substrate layer further comprising a second electronic device 30, and wherein the electronic structure further comprising: a second damascene conductive wire/stud having a lower portion in the first insulative layer and an upper portion above the first insulative layer, wherein the lower portion of the second damascene conductive wire/stud is conductively coupled to the second electronic device; and a damascene conductive wiring line 67 within the second insulative layer, wherein the damascene conductive wiring line is above the second damascene conductive wire/stud and is insulatively isolated from the second damascene conductive wire/stud; a shallow

trench isolation (STI); and an internal seam or void oriented lengthwise within the first damascene conductive wire/stud. However, Prior Art Figures 1-3E fail to teach a metallic cap. Farooq *et al.* teach a metallic caps 23 (having a preferred thickness of about 0.100 to 1.000 microns) of an electrically conductive material selected from the group consisting of aluminum, chromium, cobalt, gold, nickel, palladium, platinum, silver, to name a few that is in contact with the upper portion of a conductive wire and is different from the conductive copper stud 18; a dual damascene 28 within a second insulative layer 30 (which covers metallic cap 23) such that a dual damascene 128 is above the second metallic cap 23 and is conductively coupled to the second metallic cap; and a conductive wiring line structure 131 is above and in contact with metallic cap 23 (Figures 4-5, cols. 4-5, lines 9-67 and 1-36, respectively). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Prior Art Figures 1-3E with the metallic cap of Farooq *et al.* to reduce process variability."

Applicants respectfully contend that claim 1 is not unpatentable over related art Figures 1-3E in view of Farooq, because claim 1 as amended claims a passivating layer, a first insulative layer, and a second insulative layer. Applicants maintain that the Examiner's argument in the Office Action mailed 06/05/2002, based on related art Figures 1-3E, is inconsistent with a passivating layer, a first insulative layer, and a second insulation layer in conjunction with the following feature of claim 1: "a first damascene conductive wire/stud having a lower portion in the first insulative layer and an upper portion above the first insulative layer". Thus, Applicants

respectfully maintain that claim 1 is not unpatentable over related art Figures 1-3E in view of Farooq e*t al.*, and that claim 1 is in condition for allowance. Since claims 2-14 depend from claim 1, Applicants respectfully contend that claims 2-14 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicant respectfully contends claims 1-14 and 29-42, and the entire application are in condition for allowance. If the Examiner believes that anything further is necessary in order to place the application in better condition for allowance, the Examiner is requested to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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Appendix A. Identification of Amended Material

Please amend claim 1 as follows:

1. (AMENDED) An electronic structure, comprising:

a substrate layer that includes a first electronic device;

a passivating layer on the substrate layer and in mechanical contact with the substrate layer, wherein the passivating layer is on the first electronic device and is in mechanical contact with the first electronic device;

a first insulative layer on the [substrate layer] passivating layer and in mechanical contact with the passivating layer;

a first damascene conductive wire/stud having a lower portion in the first insulative layer and an upper portion above the first insulative layer;

a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud and in conductive contact with the first damascene conductive wire/stud;

a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and

a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive wiring line structure is above the subtractive etch metallic cap and is conductively coupled to the subtractive etch metallic cap.